Overview of ASIC Tests for Forward Pixels

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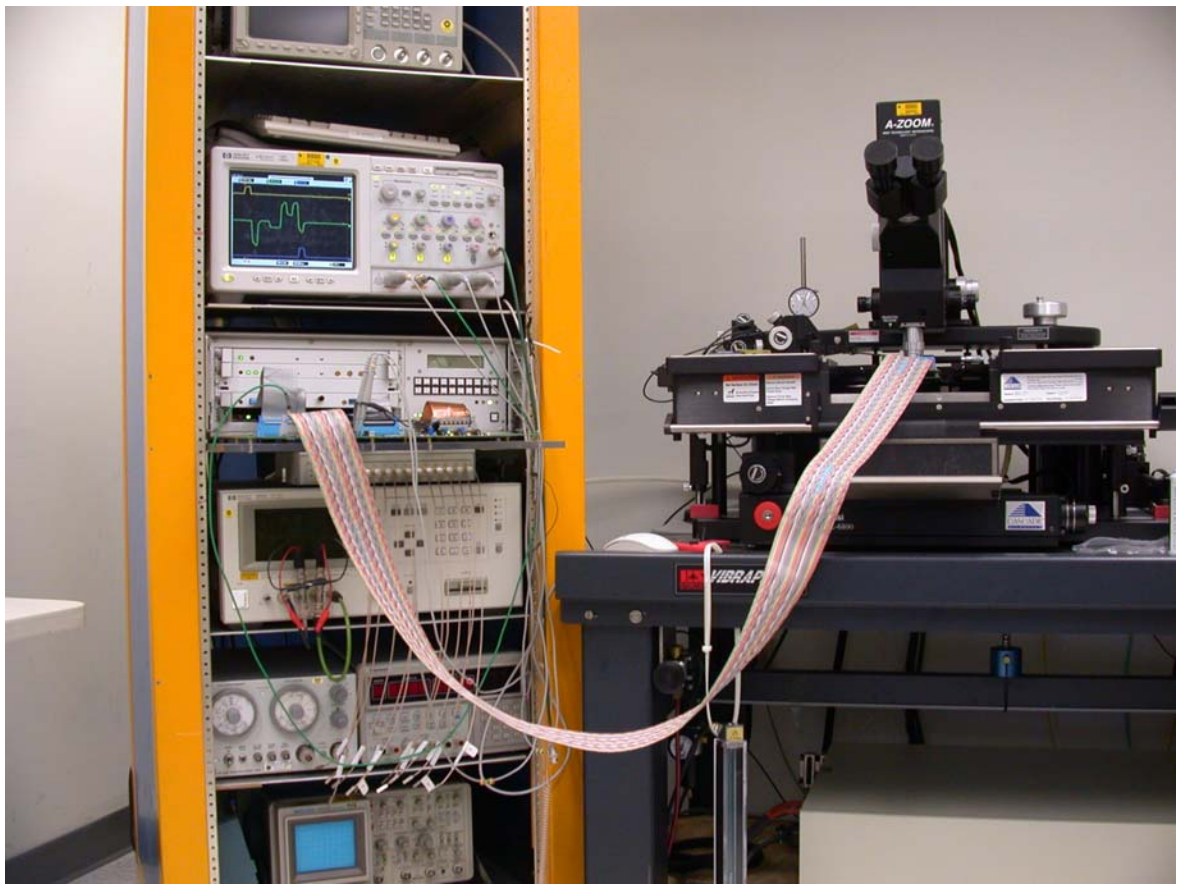
Introduction

- **Custom design chips used in Forward Pixel:**
  - ReadOut Chip (ROC) – developed by PSI
  - Token Bit Manager (TBM) – developed by Rutgers University
  - Auxiliary chips: Gatekeeper, Reset, Fan-In and Fan-Out – developed by Rutgers University
- **Tools used for chip testing:**
  - Cascade/Alessi 6171 8” chuck probe station
  - EED ASIC Test System
  - *Custom designed hardware*
  - *Custom designed software*

Hardware for ASIC testing

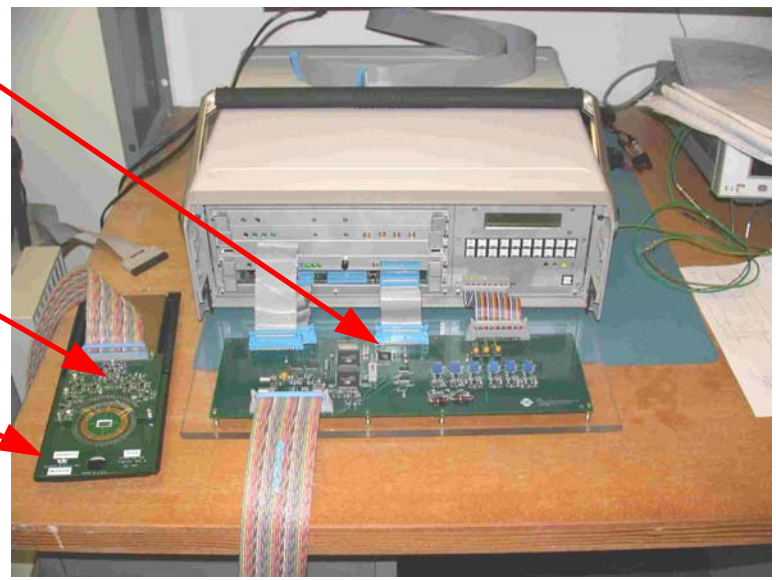
EED Wafer Test Stand with PSI46v2 Under Test



Hardware for ASIC testing

Wafer Test Stand components (see new developed designs in *green Italic*):

- EED Cascade/Alessi 6171 semi-automatic 8 inch chuck probe station
- EED ASIC Test System
- *ASIC Interface Board*
- *Buffer Board*
- *Probe card*



Readout Chip History

Readout Chips Tested at Fermilab:

- **PSI43 – tested in February 2003**
  - Very difficult chip to work with
  - Required manual adjustment of Vref
- **PSI46v1 – tested in March 2004**
  - Much better uniformity
  - No charge output
  - Oscillations of internal voltage regulators
- **PSI46v2 – tested in July 2005**
  - Production version

ReadOut Chip

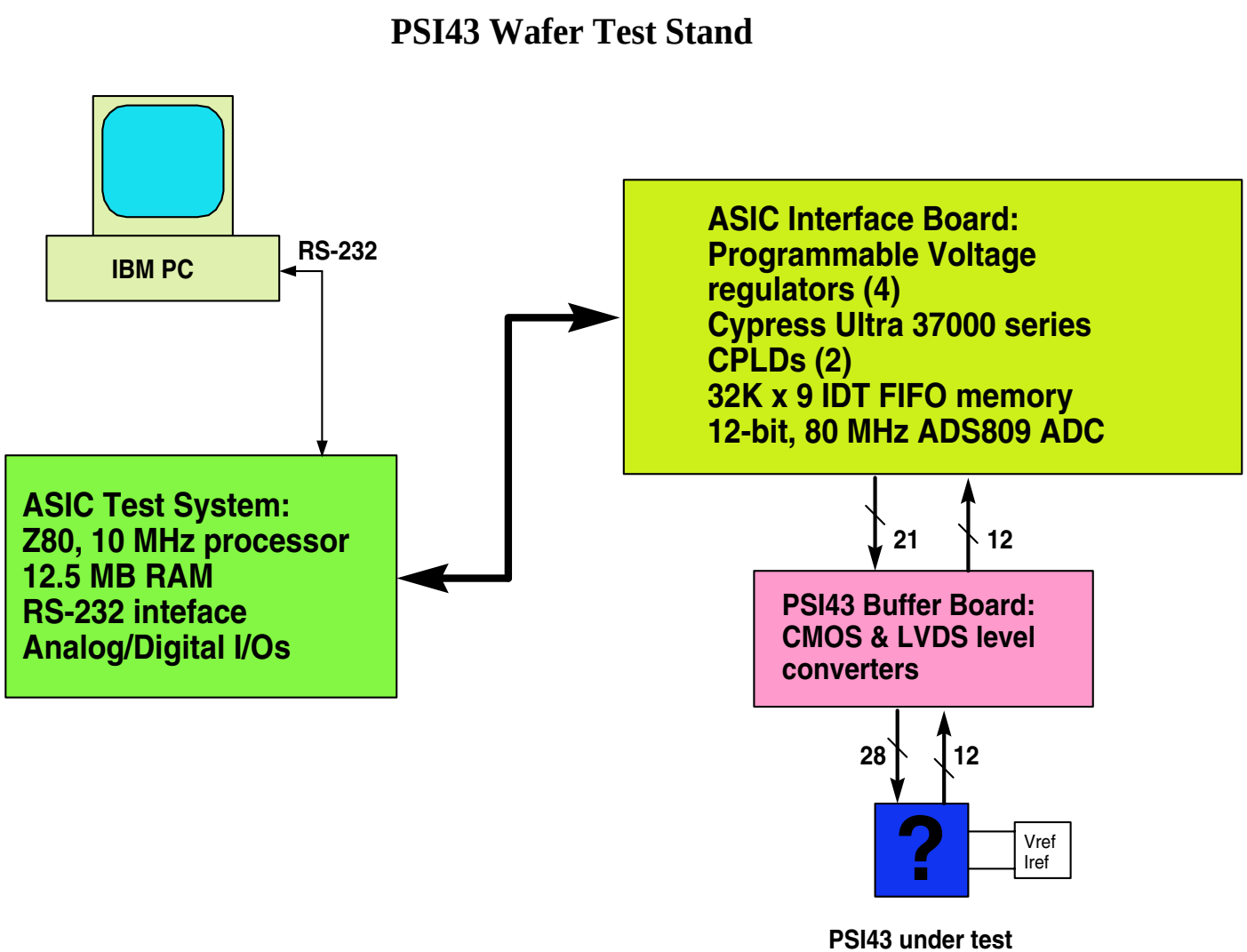
- Developed by Paul Scherrer Institute (PSI), Switzerland
- ROC went through numerous prototype stages and fabrication processes (Honeywell, DMILL, IBM)
- Current version of the chip – PSI46v2 – has been announced as a final one
- ROC designed to pick up signals from 4160 (52x80) 100 x 150 microns silicon pixels
- ROC is mainly an analog chip: output signal is a 40 MHz train of level encoded steps
- ROC has digital serial control interface working at 40 MHz clock frequency
- ROC has been tested by EED ASIC Test Group (C.Gingu and W.Wester) since version PSI43 (DMILL)

ReadOut Chip

Main ReadOut Chip parameters:

- CMOS technology – IBM 0.25μ, bulk, 5 metals
- Die size – 7900μ x 9800μ
- Number of pixels – 52 x 80 = 4160
- Pixel size – 100μ x 150μ
- Number of transistors – 1,280,000
- Number of pads – 35 (175μ pitch)
- Number of external capacitors – 2
- Supply voltages – +2.5V, +1.75V
- Supply current ~50..70mA (total)

Hardware for testing ROC



Hardware for testing ROC

ASIC Interface Board features:

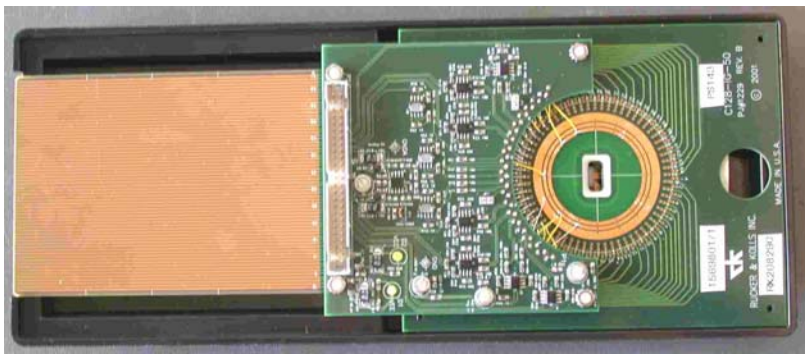
- Programmable power supplies with shutdown
- Serial command interface with two modes of operations:
  - Single command
  - FIFO command stream
- Timing generator with programmable Calibrate and Trigger pulses
- 12 bit, 40 MHz ADC for sampling analog data
- DC voltage and current measurements
- Scope outputs for trigger and analog data signals

Hardware for testing ROC

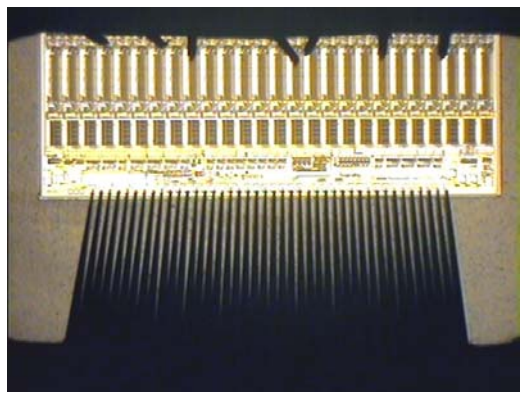
Buffer Board features:

- Level converters from standard CMOS and LVDS to negative CMOS and negative LVDS levels (for PSI43)
- True differential analog buffer amplifiers for transferring analog signals via 6 ft. twist-n-flat 3M cable

PSI43 Buffer Board (v.1)



PSI43 Probe Card



Evolution of the Design

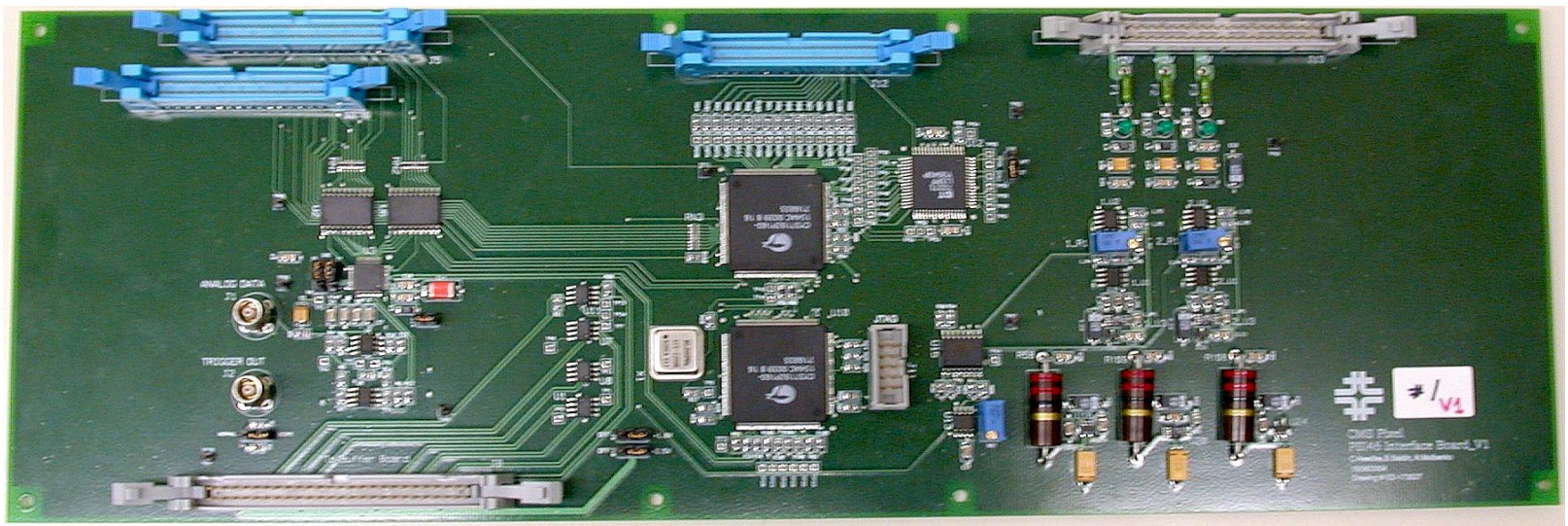
PSI43 (DMILL):

- **ASIC Interface Board v.1**
  - Four negative power supplies – (-5V, -3.5V, -3V, -2.5V)
  - Mainly 20 MHz operations
- **Buffer Board v.1**
  - Mounted on the top of a standard Rucker & Kolls probe card – non-removable
- **Probe Card**
  - Standard (for DC testing) probe card with custom wire probes

Evolution of the Design

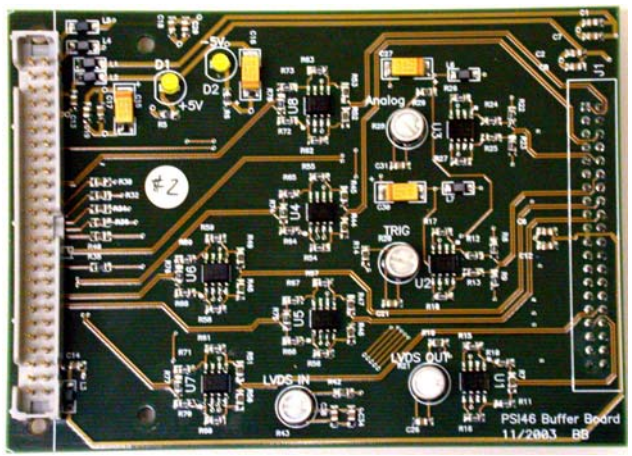
PSI46 (IBM):

- **ASIC Interface Board v.2**
  - Modified to provide only two programmable positive power supplies (+2.5V, +1.75V)
  - Modified to allow 40 MHz operations of the serial control interface using system clock

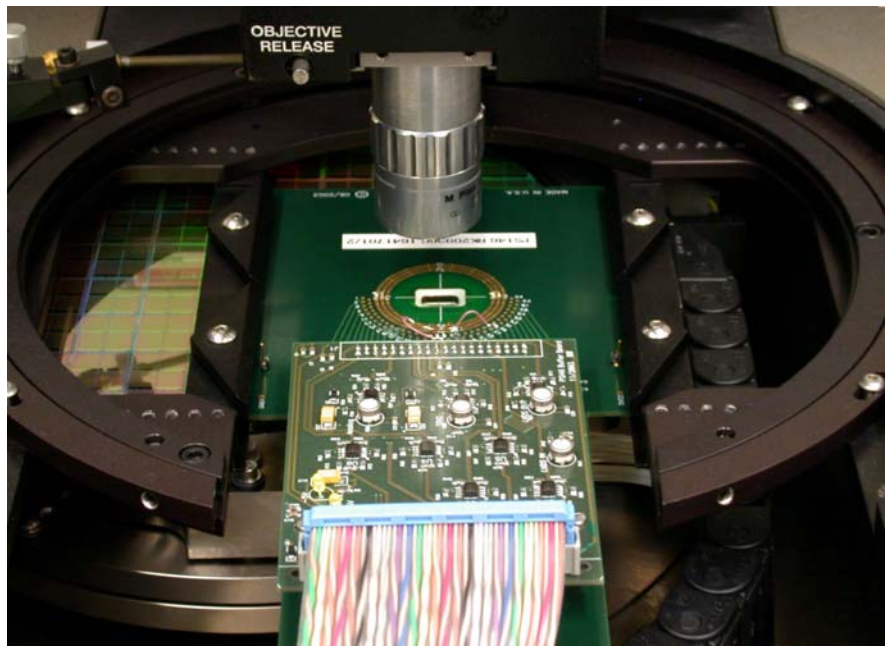


Evolution of the Design

- **Buffer Board v.2**
  - Connected to a custom high speed probe card via 40 pin IDC connector, which allows easy removal for repair



Top view of the Buffer Board



Buffer Board assembled with probe card

Evolution of the Design

- **PSI46 high speed probe card**
  - Custom probe card specified to work at 40 MHz and with up to 64 pads

Evolution of the Design

- **PSI46 Adapter Board with PSI46v2 chip**
  - Used for software and hardware debugging and reference

ROC Testing Procedure

Based on testing algorithm provided by PSI

- Interface Board setup
- Power up PSI46 chip
- Measure power supply currents and voltages
- Download chip configuration
- Measure power supply currents and voltages
- Token Out test
- Serial Interface test
- *I-V* curve test for *Va* voltage regulator (Ia=24 mA)
- DAC registers' linearity test
- Vcal and MaskTrim loop test for each of the 4160 pixels
- Data buffer test for each double column
- Time stamp buffer test for each double column @5MHz
- WBC test

ROC Testing Procedure

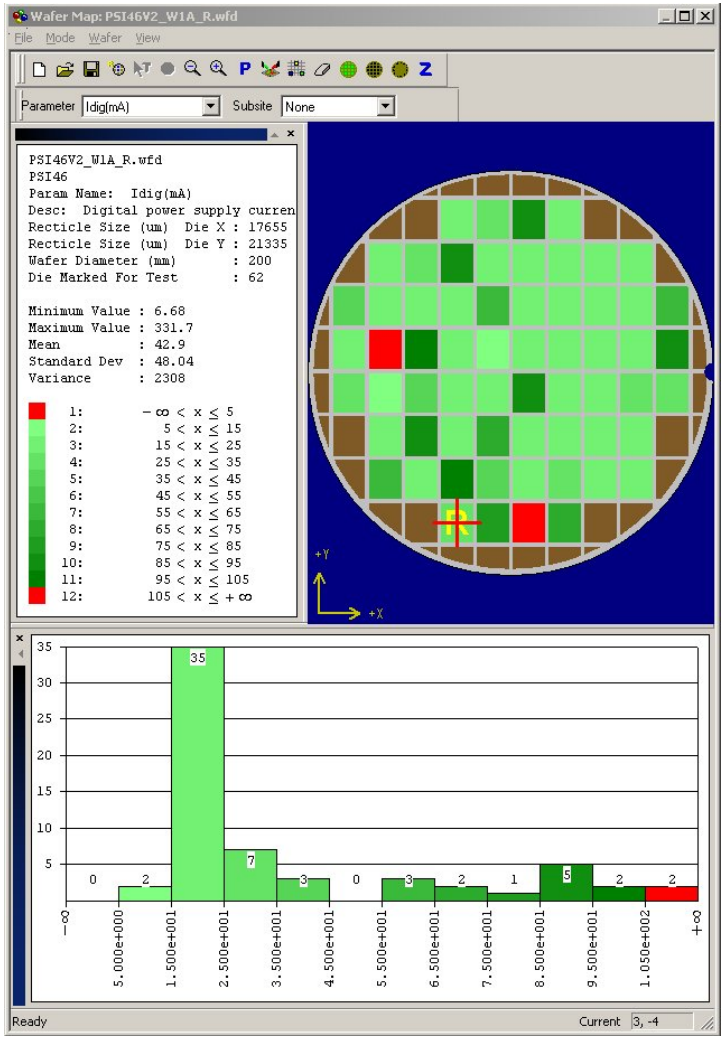
Test abort criteria:

- Ia or Id more than 105 mA or less than 5 mA
- Token Out test failed

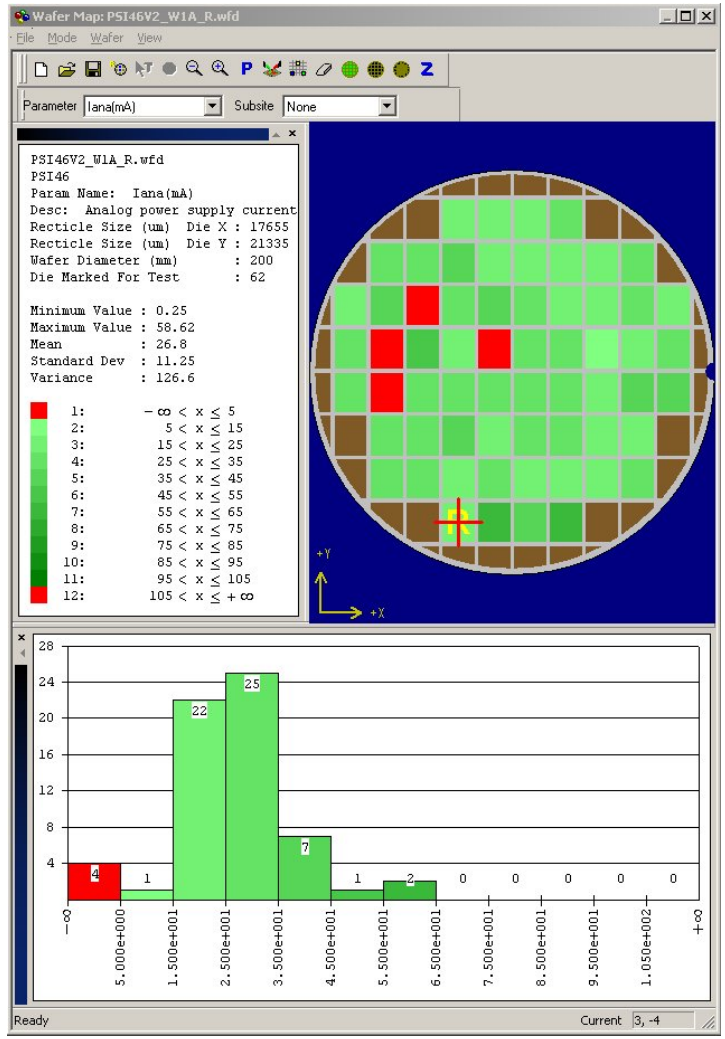
Fermilab wafer test features:

- 40 MHz instead of 10 MHz operations at PSI
- Digitization of the analog output
- Software control of the tests
- Test time ~ 3 minutes per chip:
  3x248 ~ 12 hours per wafer
- Disagreement with PSI results reduced from 6.5% to 4.4% and from 10.9% to 7.6% at 20 MHz

Test Result Examples

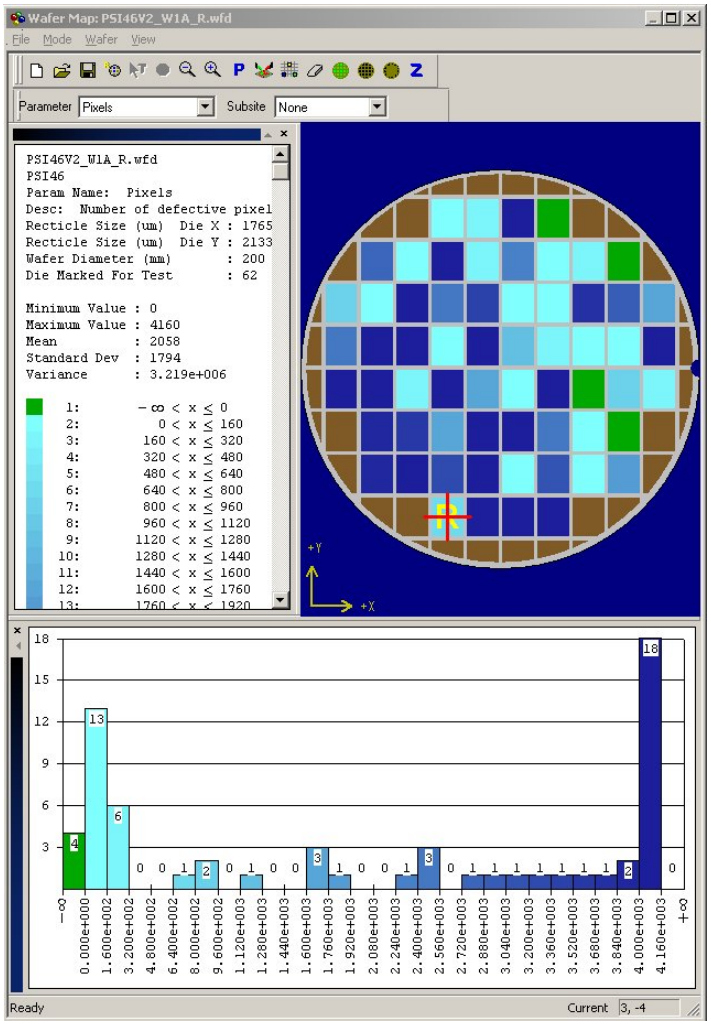


Id distribution, Wafer K7MWH6T Chip A

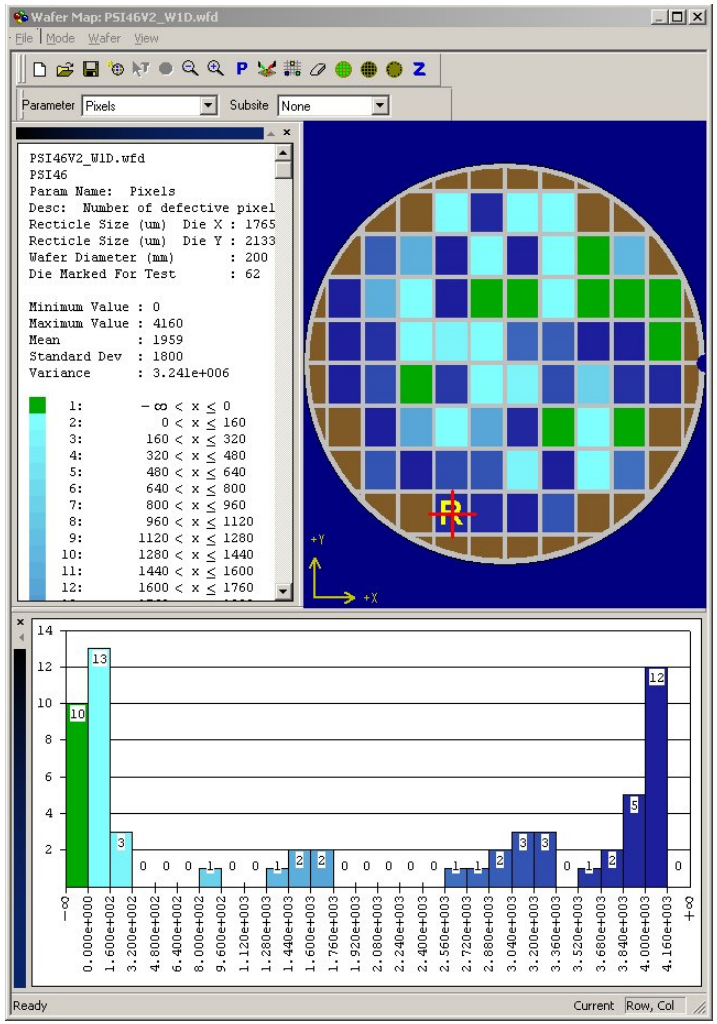


Ia distribution, Wafer K7MWH6T Chip A

Test Result Examples

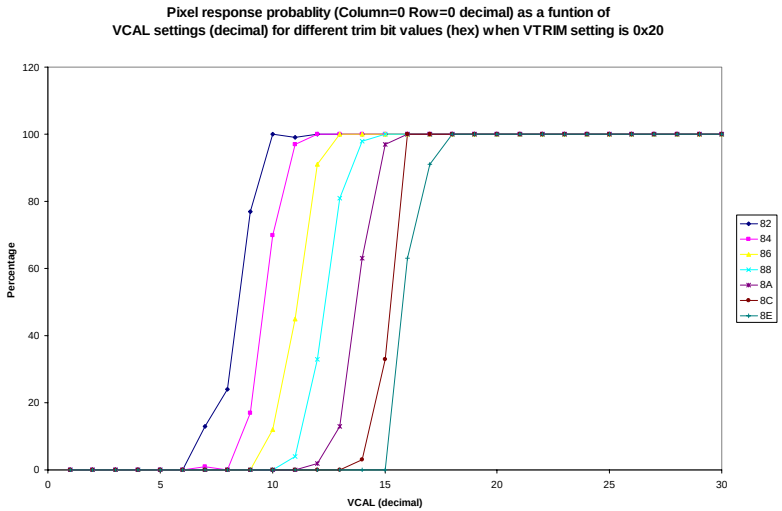


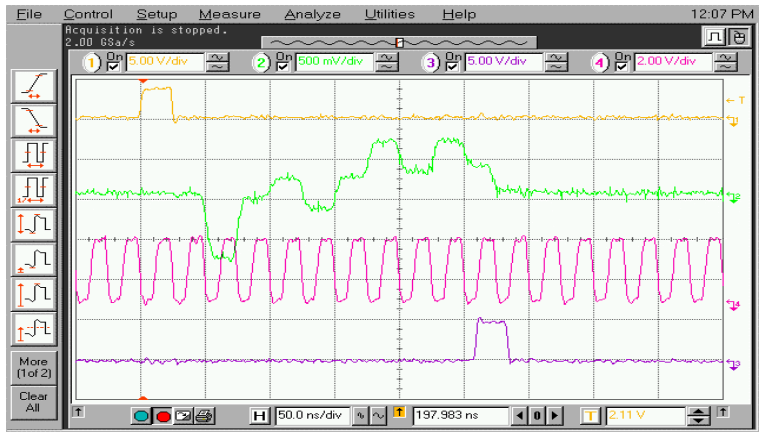
Wafer K7MWH6T Chip A defects



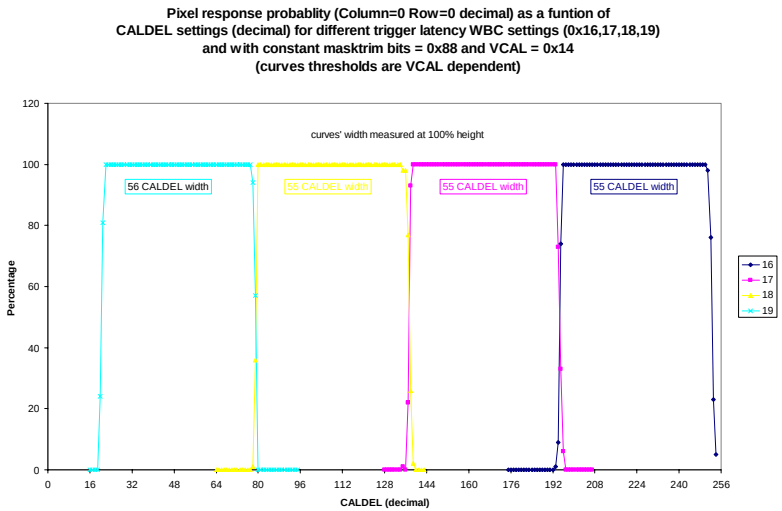
Wafer K7MWH6T Chip D defects

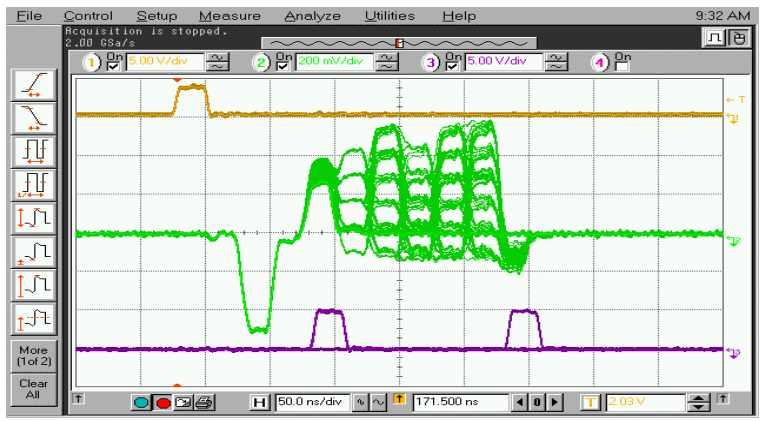
Test Result Examples





Single hit response





Accumulated all pixels response

Token Bit Manager

- Developed by Rutgers University, USA
- TBM went through similar stages as ROC from DMILL to IBM 0.25µ process
- TBM main function is to control a chain of ROCs
- TBM is mainly digital chip, but it has an analog mixer and an output similar to the ROC
- TBM uses the same serial control interface as the ROC
- TBM04 and TBM05 have been tested by EED ASIC Test Group (C.Gingu, W.Wester) as well

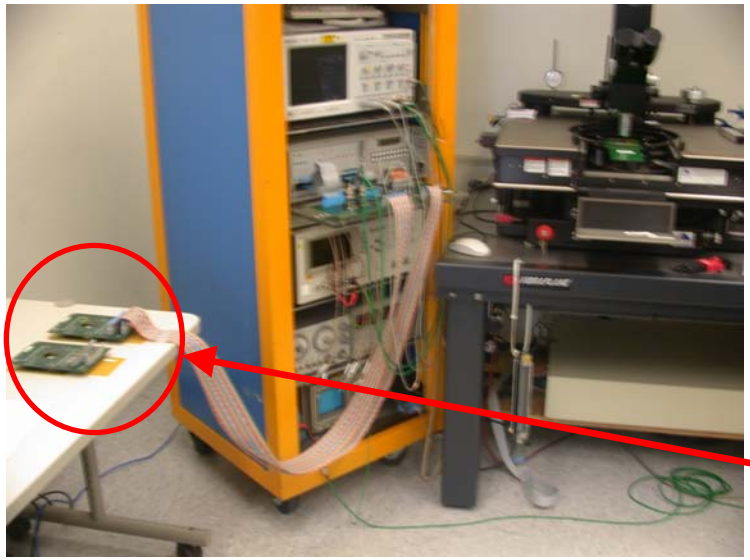
Token Bit Manager

Main TBM parameters:

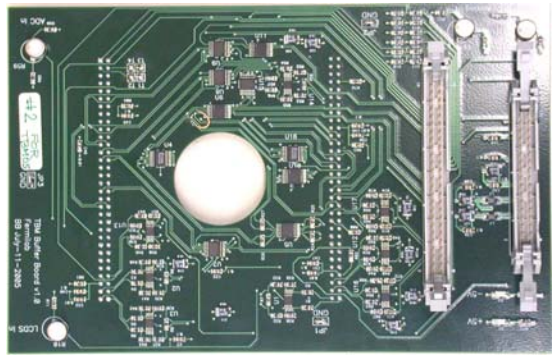
- CMOS technology – IBM 0.25µ, 3 metals
- Die size - 4800µ x 3200µ
- Number of pads – 78 (175µ pitch)
- Supply voltage – +2.5V
- Power consumption – 42.5 mW
- Dual TBM design for two readout chains up to 24 ROCs each
- Control Network HUB to separate TBM internal commands from ROC commands
- Serial control interface has read back feature as oppose to the write-only ROC registers

Hardware for Testing TBM

Details of the TBM Test Setup

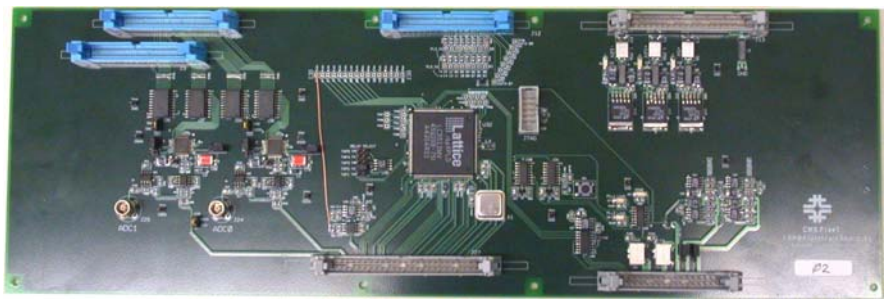


Test setup with TBM05 on adapter board



TBM Buffer Board

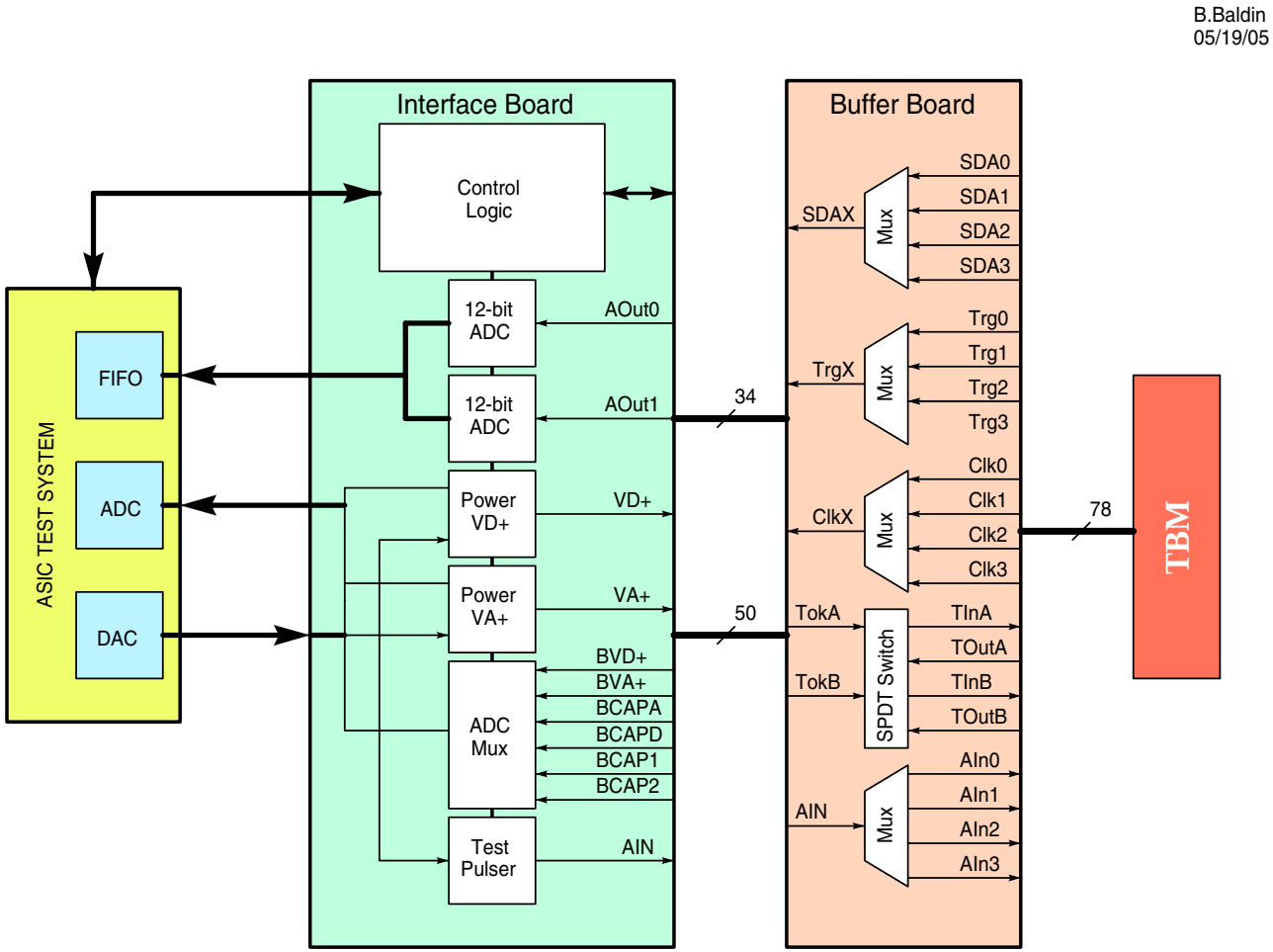
Buffer Board on top of the TBM Adapter Board



TBM Interface Board

Hardware for Testing TBM

Block diagram of the TBM Test Setup



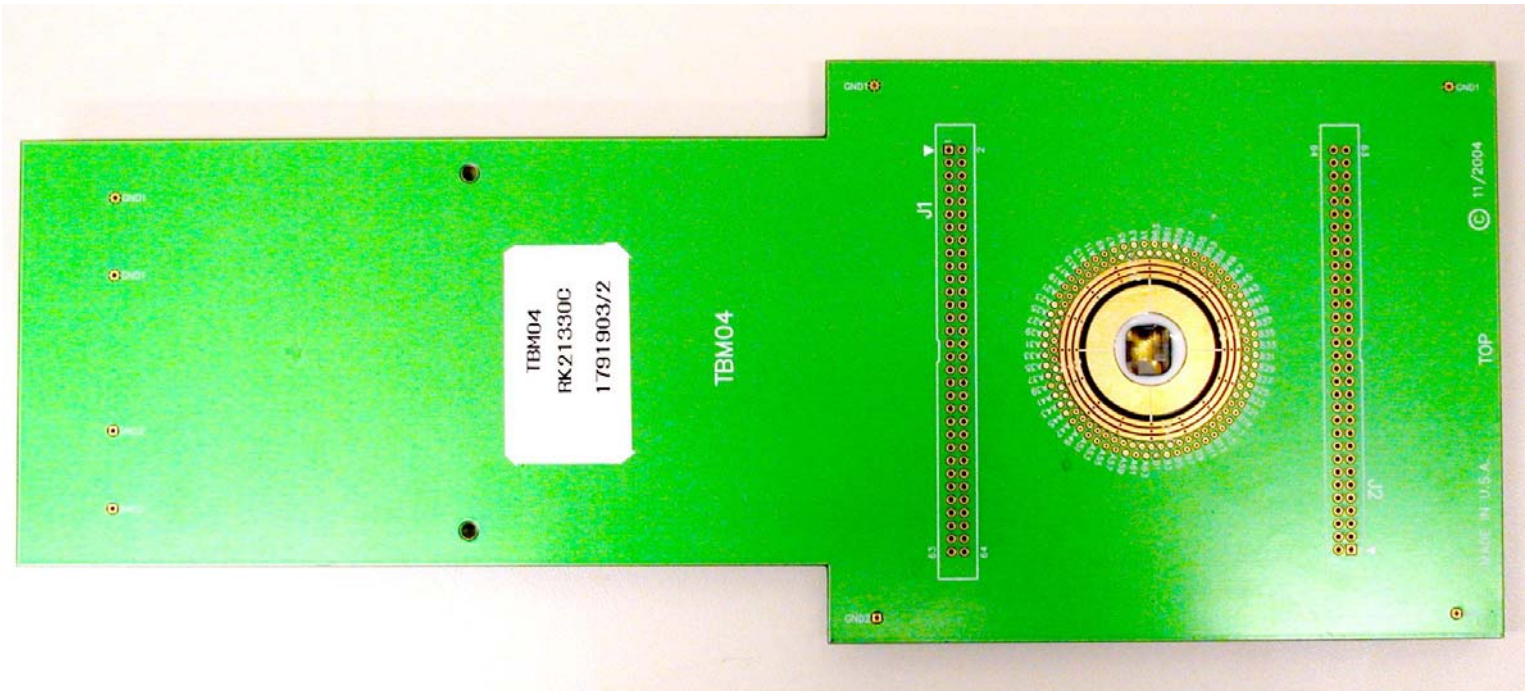
Hardware for Testing TBM

TBM Interface Board Features:

- Two programmable power supplies (Va, Vd) with shutdown
- Two 12-bit, 40 MHz ADCs for sampling analog outputs from sections A and B
- Serial command interface
- Timing generator with programmable Token, Trigger and Test pulses
- Programmable Test Pulse generator
- DC voltage and current measurements
- Scope outputs for analog data signals

Evolution of the Design

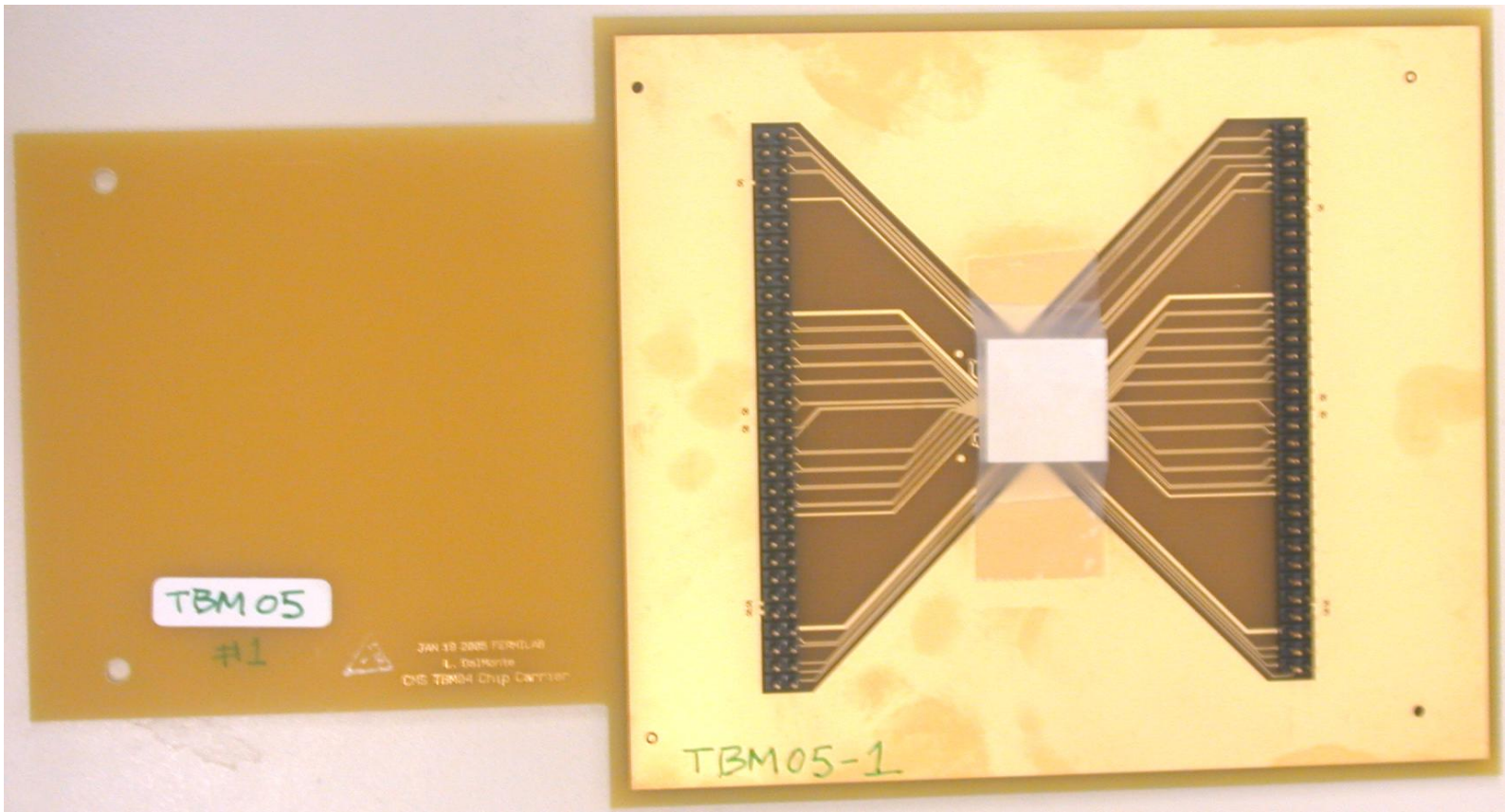
- **TBM04 high speed probe card**
  - Custom probe card specified to work at 40 MHz and with up to 128 pads



Evolution of the Design

TBM Adapter Board with TBM05 chip

- Used for debugging the system and reference



TBM Testing Procedure

TBM tests developed in cooperation with Rutgers University:

- Power supply
  - **Measure currents and voltages**
- Hub
  - **ROC ports**
  - **Hub address**
  - **TBM registers**
- TBM triggers
  - **TBM Init**
  - **CSR trigger**
  - **ROC Reset trigger**
  - **TBM Reset trigger**
  - **20 MHz readout mode**

TBM Testing Procedure

- Stack
  - **Stack content**
  - **Stack full at 24**
- Analog output
  - **TBM output gain**
  - **Analog input gain**
  - **Rise/Fall times**
  - **Linearity**
- Single TBM
  - **TBM A**
  - **TBM B**
- Miscellaneous
  - **Ignore incoming trigger**

TBM Testing Procedure

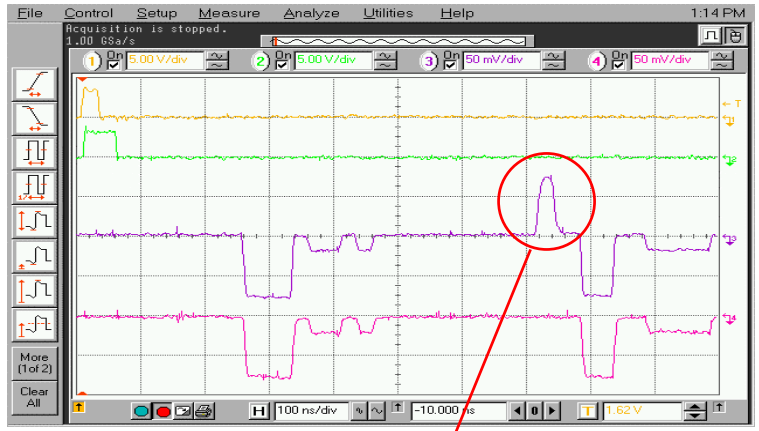
- **Disable trigger**
- **Inject software trigger**
- **Clear stack counter**

Test pass criteria (test aborted if any condition below is not satisfied):

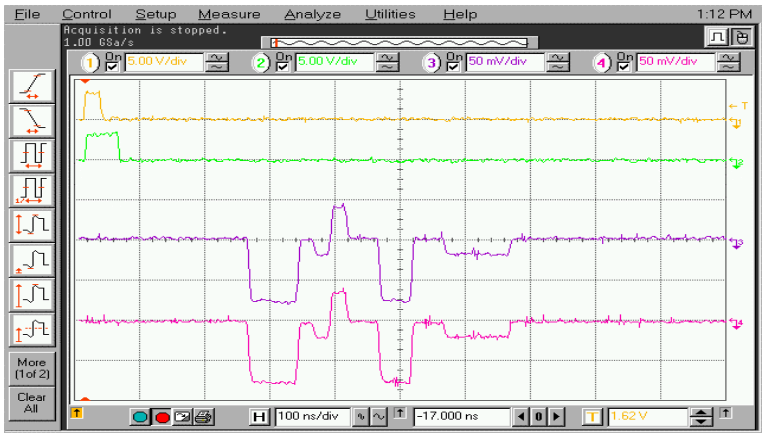
- Id is within 5 mA to 15 mA
- Ia is within 5 mA to 15 mA for TBM04
- Ia is within 10 mA to 25 mA for TBM05
- Va is within 1.8V to 2.4V
- Vd is within 1.8V to 2.4V
- Vlvdsl is within 0.7V to 1.3V
- Vlvdsh is within 0.9V to 1.5V

Test Result Examples

TBM output @20 MHz with all event counter levels



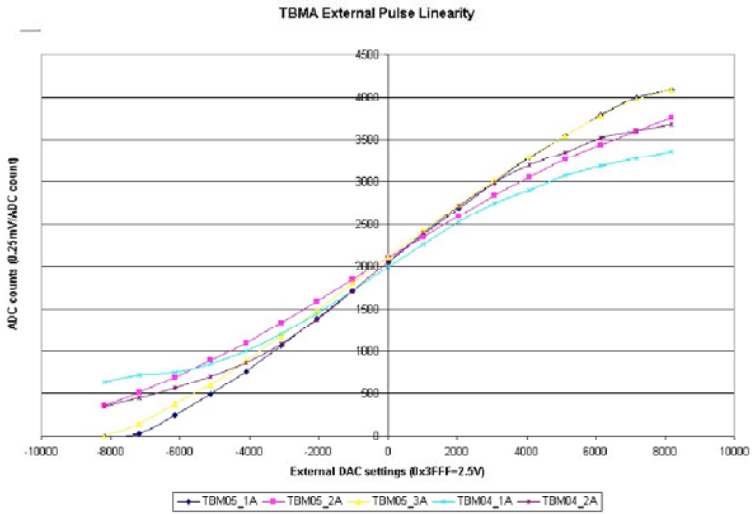
Test pulse injected between header and trailer



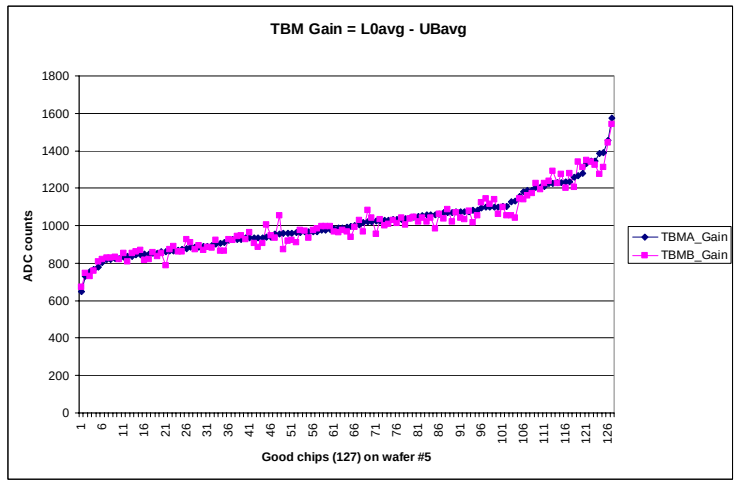
TBM outputs A and B in Token Loop Back mode

Details of the test pulse measured in closed loop

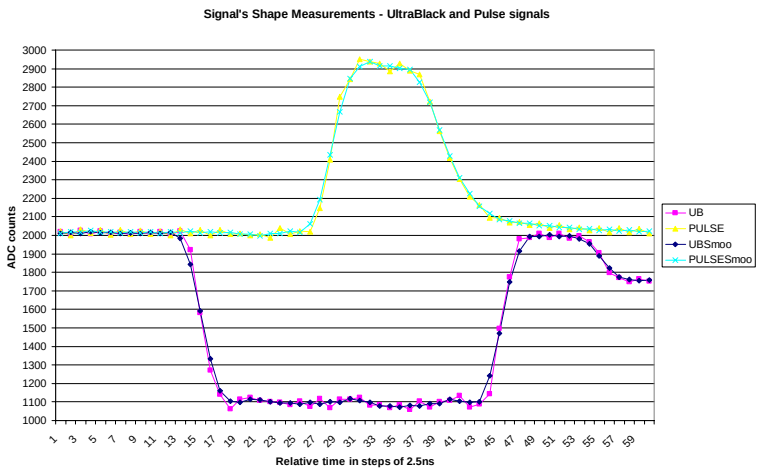
Test Result Examples



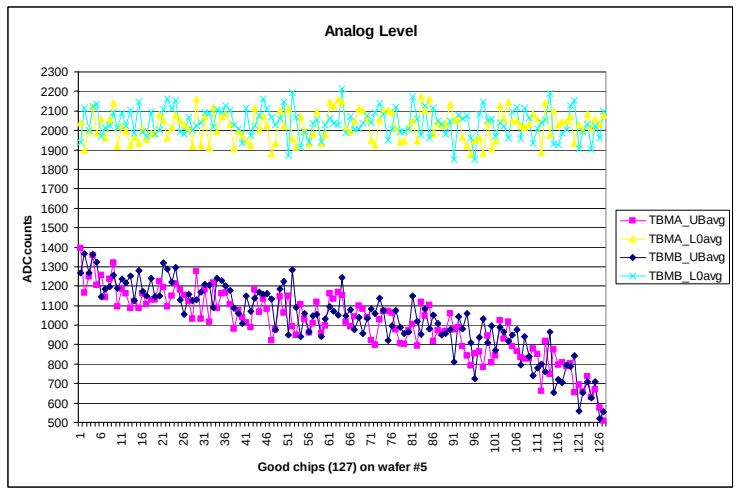
Comparison of TBM04 and TBM05 linearity



TBM05 gain variations



Rise/Fall time measurements based on ADC output



Variations of UB and baseline levels for TBM05

Auxiliary Chips

Four types of packaged chips will be tested:

- **Reset fan-out chip – CMOS level 1:6 fan-out in 16-lead 3x3 mm LPCC package**
- **Fan-In chip – differential LCDS level 6:1 fan-in in 16-lead 3x3 mm LPCC package**
- **Fan-Out chip – differential LCDS level 1:6 fan-out in 16-lead 3x3 mm LPCC package**
- **Gatekeeper chip – LVDS/CMOS inputs, LCDS inputs/outputs in 32-lead 5x5 mm LPCC package**

Auxiliary chips hardware

Auxiliary chips Interface Board features:

- Four sockets for manual placement of each type of the chip
- 40 MHz clock operations
- Pass/Fail, Power ON, DUT LED indicators

Conclusions & Future Plans

PSI46v2

- ROC Wafer Test Stand hardware successfully tested and ready for production testing
- RS-232 speed may be the limiting factor in the wafer tests
- Additional test procedures may be necessary for charge output

TBM05:

- TBM Wafer Test Stand hardware successfully tested and ready for production testing
- Selection criteria has to be finalized for production testing

Conclusions & Future Plans

Auxiliary chips:

- Completed schematic design
- PCB layout in progress
- Firmware design started
- Hardware ready by the beginning of November 2005